Ballistic Transport in Semiconducting Carbon Nanotubes

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Abstract. We report on electronic transport in devices consisting of individual semiconducting singled-walled carbon nanotubes (SWNTs) grown by a chemical vapor deposition technique and contacted by metal electrodes. Low-temperature electronic transport at negative gate bias indicates the SWNTs act as single quantum dots with a length on order of the electrode spacing, indicating that the mean free path is greater than the contact spacing (~1μm). Upon increasing gate bias, an intermediate multiple quantum dot regime is observed, followed by a gapped region at positive gate bias. At room temperature and zero gate bias a mean free path of 700nm is determined using electrostatic force microscopy to probe the local potential in the SWNT.

Ballistic electronic conduction has been observed in metallic single-walled carbon nanotubes (SWNTs) [1], but the electronic transport in semiconducting SWNTs has been reported as consistent with tunneling through a series of closely spaced (~100nm) low transmission conduction barriers [2]. The SWNTs in the above studies were prepared using a laser vaporization technique, with subsequent treatment in an ultrasonic bath in order to separate individual SWNTs from bundles. Here we report measurements on individual semiconducting SWNTs prepared directly on insulating SiO_2 substrates by chemical vapor deposition (CVD). These semiconducting SWNTs show long mean free paths, up to 700nm at room temperature, and over 1μm at 1.5K.

Following the method of Kong, et al. [3], catalyst islands were patterned on a substrate consisting of heavily doped conducting Si capped with 1μm of SiO_2. SWNTs were grown by flowing methane over the substrate and catalyst at 900ºC. After growth, SWNTs were located relative to pre-patterned alignment marks using a field-emission-filament scanning electron microscope operating at 1kV accelerating voltage. A second electron beam lithography step was used to define metal (Cr/Au) contacts to selected SWNTs. The above method of device fabrication produces both metallic and semiconducting SWNT devices. The two-terminal conductance as a function of voltage applied to the gate electrode (conducting substrate) is used to determine whether each device is metallic or semiconducting as follows. The conductance of the metallic SWNT devices is nearly independent of gate voltage, while the conductance of the semiconducting devices decreases as the gate voltage is increased (see fig. 1), indicating p-type conduction [4].

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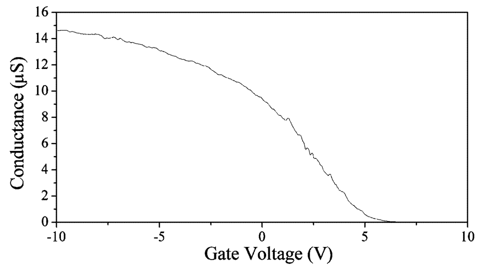

FIGURE 1. The conductance of a typical semiconducting single-walled carbon nanotube device as a function of gate voltage at T=290K. The SWNT has a diameter of 0.9 nm and a length of 1.06 μm.

The low-temperature electronic transport through SWNT devices is typically dominated by Coulomb charging effects. In metallic SWNT devices, the data are often consistent with transport through a single quantum dot with length equal to the length of the SWNT [5-7]. Semiconducting devices typically show a gap for electronic transport at low bias, which has been interpreted in terms of multiple quantum dots created by large tunnel barriers along the length of the nanotube [2].

Figure 2 shows a series of greyscale plots of conductance as a function of source-drain voltage and gate voltage for a semiconducting SWNT device at a temperature of 1.5K. In Figure 2a, in the negative gate voltage regime (high doping), regular oscillations of the conductance with gate voltage are observed, with a period $\Delta V_g \approx$ 20mV. An oscillatory gap in the conductance as a function of source-drain voltage of approximately 2-3mV (half width half maximum) is also observed.

We will attempt to understand these features in terms of Coulomb blockade. It was previously found for metallic SWNTs with similar geometry that the Coulomb charging energy $U = e^2/C$ = (3-7meV)/L, where L is the distance between electrodes in microns [5-7]. The period of oscillation in gate voltage depends on the coefficient $\alpha = C_g/C$, where C_g is the capacitance of the dot to the gate electrode, and C is the total capacitance of the dot. For devices of this geometry, α is typically about 0.1 [7]. The period in gate voltage is given by $\Delta V_g = (U + \Delta E)/e\alpha$, where ΔE is the energy level spacing. $\Delta E \ll U$ for a semiconducting dot, due to the high density of states at the band edge [8]. Therefore, $\Delta V_g \approx U/e\alpha \approx$ (30-70meV)/L.

The Coulomb charging energy U $\approx$ 2-3meV and gate voltage periodicity $\Delta Vg \approx$ 20meV imply a dot of length L $\approx$ 1.5-3.5μm. This is somewhat longer than the contact spacing in this device (1.06μm), indicating that the relevant length may include some of the SWNT under the electrodes. In any case, the observation of conductance oscillations with a single well-defined period, and the small Coulomb gap in this device strongly suggest that the transport is coherent at least over the electrode separation distance of ~1μm at low temperature and negative gate voltage.

As the gate voltage is increased, the SWNT is depleted of holes (see Figures 2b and 2c). The small charging gap evident at negative gate voltages becomes larger, and eventually there is no conductance at zero bias. While the conductance oscillations

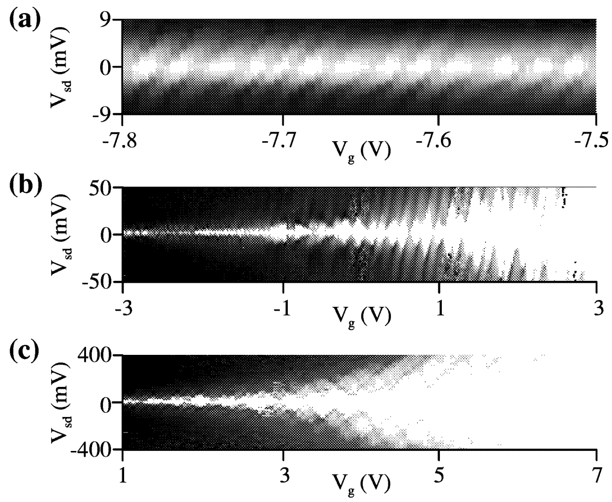

FIGURE 2. Greyscale plot of differential conductance of a semiconducting single-walled carbon nanotube device (same device as fig. 1) as a function of source-drain bias and gate voltage. White represents zero conductance and black high conductance (~10μS).

at positive gate voltage are more irregular, some regions with a single dominant period are evident; for instance, a period $\Delta Vg \approx 140$mV is observed for $0V < V_g < 1V$, and a period $\Delta Vg \approx 400$mV is observed for $3V < V_g < 5V$, corresponding to quantum dots of length roughly 400nm and 100nm respectively. We speculate that as the SWNT is depleted of holes, discrete areas of high local electrostatic potential become transport barriers, and the SWNT breaks up into a series of dots. Sometimes one dot dominates the transport, and this leads to a dominant period in the conductance as a function of gate voltage. It is notable that the SWNT is apparently not completely depleted of holes for gate voltages as high as +7V.

Electrostatic force microscopy (EFM) was used to determine the local potential in a current-carrying SWNT at room temperature. The EFM experiments were carried out on a semiconducting SWNT device measuring approximately 5μm between electrodes. In addition, scanning-gate microscopy (SGM) was used to image local conduction barriers in the SWNT. The EFM and SGM measurements were made using a conducting tip atomic force microscope (AFM); details are described elsewhere [1].

Figure 3a shows a topographic AFM image of the semiconducting SWNT device. The SWNT has a diameter of 2.0nm, and a two-terminal resistance of 143kΩ at zero gate voltage. Figure 3b shows an SGM image of the same device; here the AFM tip is held at a –1V relative to the SWNT while it is scanned over the sample. The image shows the change in resistance of the sample; dark spots indicate a decrease in resistance. The darkest spots correspond to approximately 500Ω change in resistance,

(a)

(b)

(c)

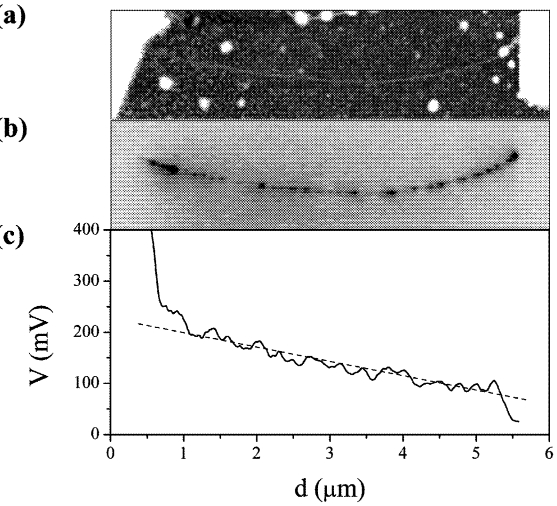

FIGURE 3. An atomic force microscope image of a semiconducting single-walled carbon nanotube device is shown in (a). The large white features at each side are the Cr/Au electrodes, the thin grey line is the nanotube. A scanned-gate microscopy image (b) of the same device as in (a). The image (b) was taken with -1V applied to the tip, and 1V applied across the nanotube. Dark color indicates decreased resistance; black corresponds to a change in resistance of approximately 500 Ω. The local potential in the nanotube under an applied bias of 400mV is shown in (c). The dashed line is a guide to the eye, and represents a voltage drop corresponding to 9.2kΩ/μm. The distance scale in (c) applies to all figures.

suggesting a series of nearly transparent barriers. Figure 3c shows an EFM trace of the local potential along the SWNT with a bias of 400 mV applied to the contacts. About 32% of the voltage is dropped along the SWNT, indicating the resistance of the SWNT is about 46kΩ, or 9.2kΩ/μm. The left and right contacts have resistances of 71kΩ and 26kΩ respectively. Assuming four conducting channels (two spin-degenerate bands) in the SWNT, the resistance of a given section of the SWNT is given by $R = (h/4e2)(1-T)/T$ where T is the transmission coefficient for electrons traversing the section of SWNT. The mean free path, the length over which T = 0.5 (R ≈ 6.5kΩ), is thus 700nm for this semiconducting SWNT at room temperature.

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