

Supporting Information for

Screening-engineered Field-effect Solar Cells

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This PDF file includes:

Supporting Methods:

I.A: Simulation methods for type A cells

I.B: Simulation methods for type B cells (graphene)

II.A: Fabrication of type A cells (Si, Cu₂O)

II.B: Fabrication of type B cells (graphene)

II.C: Device testing

Supporting Discussion:

III.A: Type A and B Si cell efficiency refinements

III.B: Performance of type B “bilayer” graphene cells

Supporting Figures

Figure S1. Simulation of efficiency and V_{oc} as a function of finger separation s

Figure S2. Simulated IV curves (AM1.5 illumination) for the type A devices shown in the main text Fig. 1b

Figure S3. Schottky barrier heights as a function of gate charge for monolayer, bilayer, and many-layer graphene type B devices (corresponding to main text Fig. 1e)

Figure S4a. Experimental IV plots for type A Schottky contacts to Si

Figure S4b. Converting type A Schottky contacts to ohmic

Figure S5. Experimental IV plots for type B “bilayer” graphene (two monolayers) on n-type Si

Figure S6. Comparing self-gating and saturated gating for type A devices

References

Supporting Methods

I.A Simulation methods for type A cells

We perform simulations using COMSOL finite-elements software to solve the drift-diffusion-Poisson equations in the device structures. The simulations of finger devices are two-dimensional (assuming uniform extrusion in the third dimension), and have periodic boundary conditions to simulate an array of equally-spaced wires. The Poisson equation incorporates both the semiconductor and the gate insulator, with the three metal electrodes (gate, finger, and bottom) used to define the boundary conditions. Majority-carrier transport at the Schottky barriers is treated in the Crowell-Sze model²⁵, with the thermionic-emission barrier height taken at the semiconductor-metal interface. Image-force lowering of the Schottky barrier is taken into account by self-consistently changing the effective metal work function based on the local electric field²⁶. Notably, the image-force lowering was often zero in the nanofinger (type A) devices, due to the inverted sign of the electric field at the metal interface. Instead of modeling a back-surface field, recombination at the back contact is simply set to zero. The incident photon flux was equivalent to AM1.5, and the absorption profile was approximated by an absorption coefficient $\alpha=3\times 10^3\text{cm}^{-1}$. SRH recombination is included with a lifetime of 100 μs . Auger recombination was negligible in these structures.

I.B Simulation methods for type B cells (graphene)

Our simulation of type B graphene solves several coupled equations to describe a self-consistent system. To begin, the graphene charge Q_{gr} must equal the difference between the D-field in the gate insulator and the D-field at the surface of the silicon:

$$Q_{gr} / A = D_{gate} - D_{surf}$$

Second, the charge in the graphene alters graphene's work function:

$$\chi_{gr} = \chi_{cn-gr} + \hbar v_F |Q_{gr} / q|^{1/2} \text{sign}(Q_{gr})$$

where v_F is the Fermi velocity and χ_{cn-gr} is the work function of charge-neutral graphene (i.e., the energy to bring an electron from the Dirac point to vacuum), which we approximate as 4.6eV (assuming a Schottky-Mott band-bending relationship)²⁷. Bilayer graphene is treated as two graphene sheets, each with its own work function, in a similar self-consistent approach. Its gate-response is reduced, since the top sheet screens the bottom sheet. Graphite is treated analogously, as the limit of infinitely many sheets. In all cases the extrinsic graphene/graphite doping is assumed to be zero. For a conventional metal, even very thin, the density of states is so large that the work function is totally independent of charge state. For this reason, conventional metals would perfectly screen a gate, but graphene does so only partly. Third, the drift-diffusion-Poisson equations must be satisfied in the silicon. These equations have a boundary condition affected by χ_{gr} , and in turn determine D_{surf} . Self-consistent solutions to these three coupled conditions are found by iteration.

II.A Fabrication of type A cells (Si, Cu₂O)

Type A Si ohmic cells are produced as follows. We start with a p-type Si wafer ($N_A \sim 1 \times 10^{16} / \text{cm}^3$, B-doped) with 100nm thermal oxide. E-beam lithography (PMMA resist) is used to define alignment marks (evaporated Cr/Au), a region of exposed Si (SiO₂ etched with 5:1 BHF), and ohmic contacts (250nm wide thermally evaporated Al, 5 μm spacing, 75nm out of plane, evaporated at a slight angle to ensure continuity over the SiO₂ step). Ohmic back contacts are formed by etching the back SiO₂ with 5:1 BHF and thermally evaporating 100nm Al. At this point, the cell is annealed at 475C in 150scm Ar for 30 minutes to ensure that all Al contacts are ohmic. Finally, a gate is applied by evaporating 150nm SiO₂ and a semitransparent Cr/Au layer (1.5/12nm, respectively, which yields ~40% visible light transmission into the cell).

Type A Si Schottky cells (see Figs. S4a and S4b below) are produced in a similar fashion to the Si ohmic cells, except that the Al back contact is applied and annealed before the deposition of the top finger contact, and the top finger contact is comprised of Cr/Au (~5/50nm out of plane respectively, 300nm wide, with 5 μm spacing). Furthermore, $N_A \sim 3 \times 10^{15} / \text{cm}^3$ p-type Si is used for the Schottky cells.

Type A Cu₂O cells are produced as follows. 250 μm thick Cu foil (Puratronic, Alfa Aesar #42974) is thermally oxidized²² and mechanically polished. 750nm wide, 100nm high sputtered ITO contacts are lithographically defined, followed by gate deposition – e-beam evaporation of a 125nm MgO dielectric and sputtering of a thin (40nm) ITO contact. Ohmic contact is made to the underside of the foil using silver epoxy (Epotek H20E).

II.B Fabrication methods for type B cells (graphene)

Type B graphene on n-Si cells are produced as follows. An n-type Si wafer ($N_D \sim 10^{16} / \text{cm}^3$, P-doped) with 100nm thermal oxide is covered with PMMA resist, and a 2mm x 2mm square is

exposed via e-beam lithography. 5:1 BHF is used to etch the thermal SiO₂ within this square. Graphene is grown by low pressure CVD on Cu following a modified recent 2-stage recipe²⁸. PMMA-supported graphene is then draped over the exposed Si. The PMMA used for transfer is removed with acetone, and a copper shadow mask is then used to evaporate a Cr/Au contact to the graphene (making sure to contact the graphene only in regions where it is resting on SiO₂, to prevent direct contact between the Cr/Au and Si). An ohmic back contact is fabricated by removing the backside SiO₂ with 5:1 BHF and thermally evaporating 70nm Al. “Bilayer” samples are fabricated by repeating the monolayer graphene transfer onto existing monolayer devices (see Fig. S5).

II.C Device testing

Electrical measurements are performed using a home-built 3-point probe station with Cu pin probes. Two Keithley 2400 sourcemeters are used to apply the gate voltage and bias voltage, and an Oriel solar simulator (model #67005) is used to simulate AM1.5 sunlight.

Supporting Discussion

III.A Type A and B Si cell efficiency refinements

Monocrystalline p-type Si can have a large electron minority carrier diffusion length (L_e) on the order of 100-200 μ m, allowing photogenerated carriers to travel up to a distance L_e before being reaching the junction; in our case, the junction is the full gated region. Therefore, cell areas are effectively enlarged by L_e in all directions. For type A ohmic Si cells, the gated area is \sim 600 μ m x 600 μ m, so the true area may up to 1mm x 1mm, decreasing the effective *PCE* by a factor of 0.36, from \sim 1.4% to \sim 0.5% ($V_g=3.2$ V). For type A Schottky Si cells (Figs. S4a and S4b), the gated area is \sim 200 μ m x 200 μ m, so this effective *PCE* reduction is more pronounced. We note that the area of all of our type B cells is large enough that the hole minority carrier diffusion length (L_h) in the n-type Si does not significantly rescale our reported device efficiencies.

III.B. Performance of type B “bilayer” graphene cells

The most significant barrier to high performance in the type B monolayer graphene device (main text Fig. 4) is likely the high series resistance (R_s) of SLG. To reduce R_s , we transferred a second layer of SLG onto the device, thus creating a “bilayer” graphene top electrode. While the series resistance decreased and fill factor improved with addition of the second layer, this device was not as easily improved by gating (see Figure S5). We attribute this partly to the formation of ripples and folds in the second layer of graphene which locally inhibit the effect of the gate and act as shunt paths. A true as-grown graphene bilayer device would not suffer from these effects.

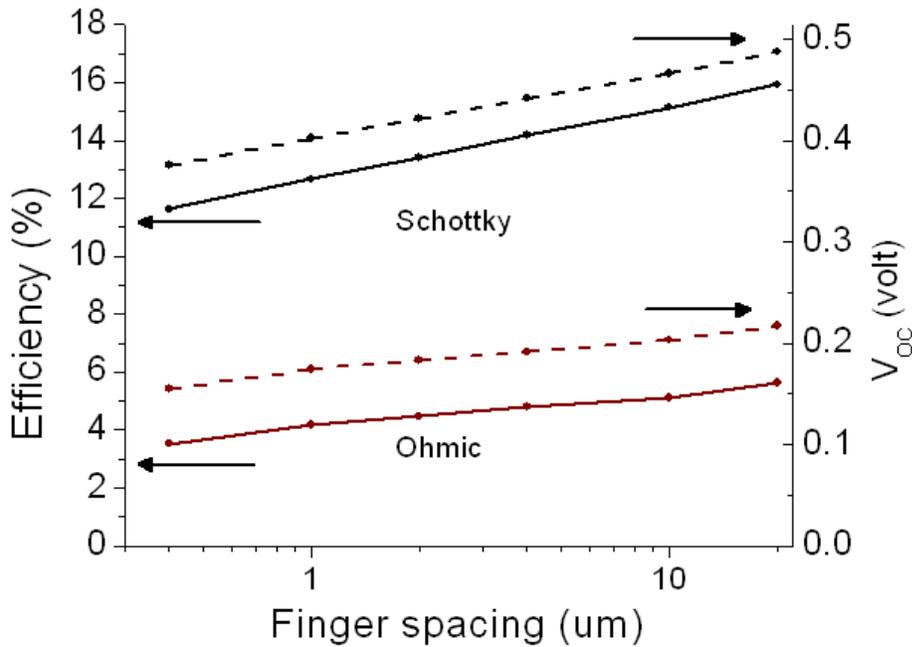


Figure S1. Simulation of efficiency and V_{oc} as a function of finger separation s . Simulations on type A cells (100nm wide Schottky nanofingers on $N_D \sim 10^{15}/\text{cm}^3$ n-type Si) with varying finger separation. Decreasing the spacing increases saturation current, particularly when the spacing becomes less than the depletion width. In practice, decreasing the spacing will also decrease series resistance but increase shading (in a top contact configuration).

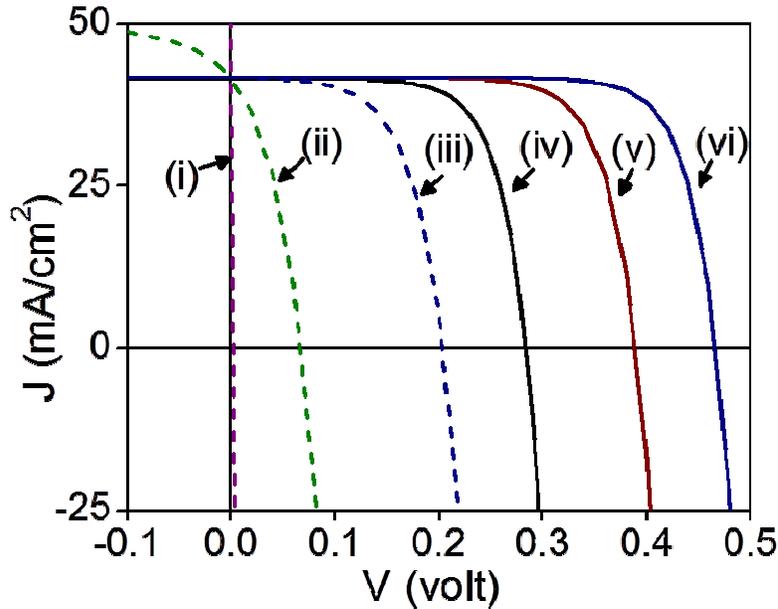


Figure S2. Simulated IV curves (AM1.5 illumination) for the type A devices shown in the main text Fig. 1b.

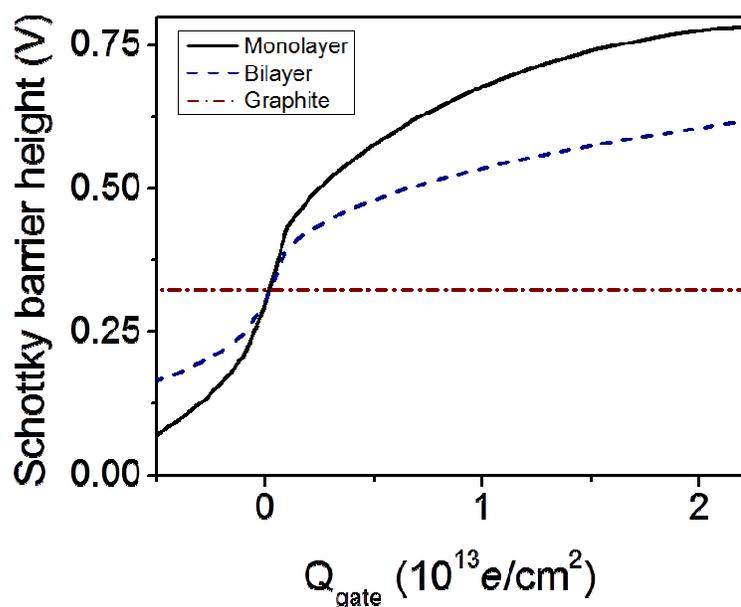


Figure S3. Schottky barrier heights as a function of gate charge for monolayer, bilayer, and many-layer graphene type B devices (corresponding to main text Fig. 1e).

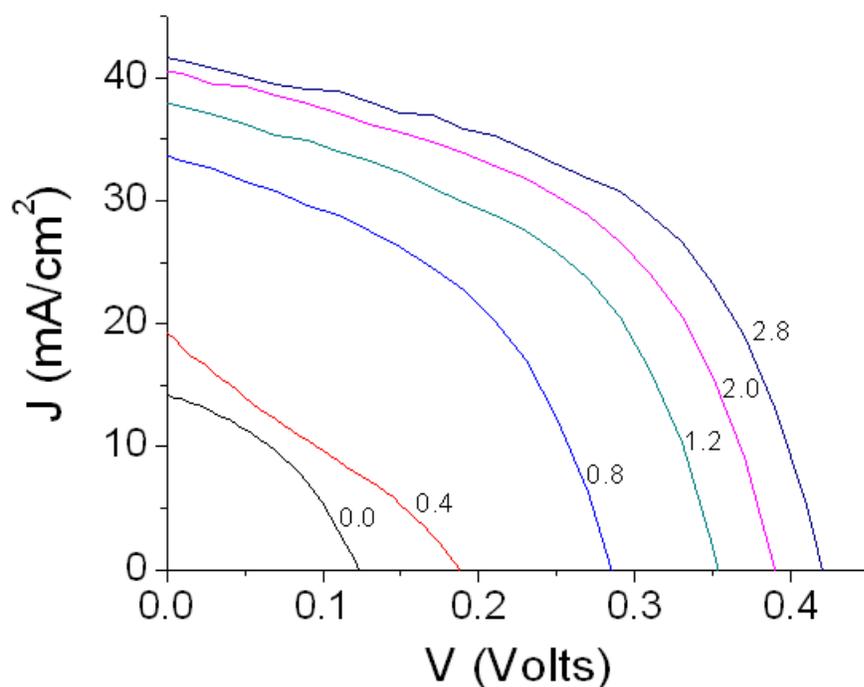


Figure S4a. Experimental IV plots for type A Schottky contacts to Si. IV plots in the positive gating regime are shown for 300nm wide Cr fingers on $N_A \sim 3 \times 10^{15}/\text{cm}^3$ p-type Si (similar to cell v in Fig. 1b in the main text). As the gate voltage (curve labels) is varied from 0.0V to 2.8V, PCE increases from $\sim 0.7\%$ to 9%. See discussion above (III.A) for adjusted device efficiencies. Illumination is AM1.5.

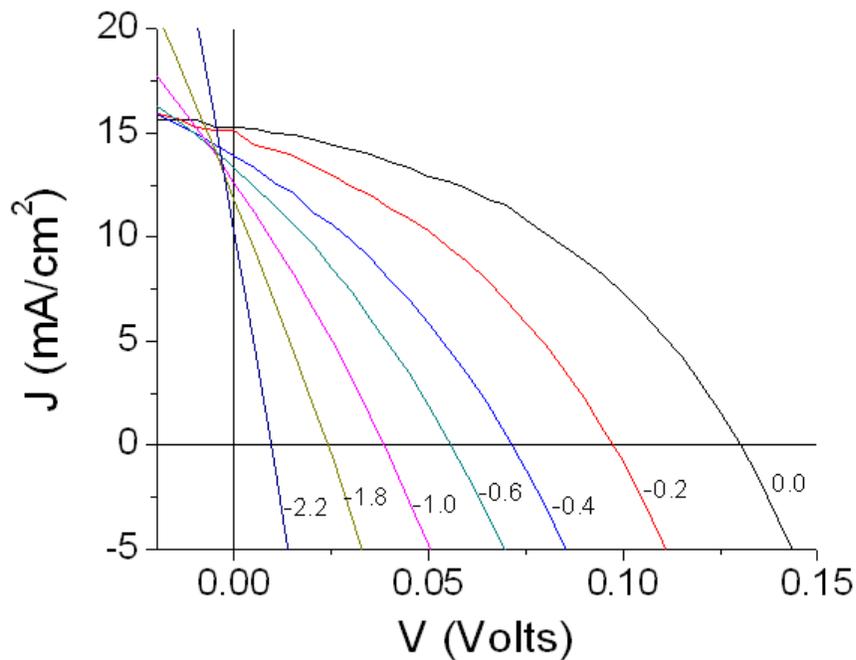


Figure S4b. Converting type A Schottky contacts to ohmic. IV plots in the negative gating regime are shown for the device in Fig. S4a. As the gate voltage (curve labels) is varied from 0.0V to -2.2V, the potential barrier at the Schottky junction is reduced, effectively creating an ohmic contact. Illumination is AM1.5.

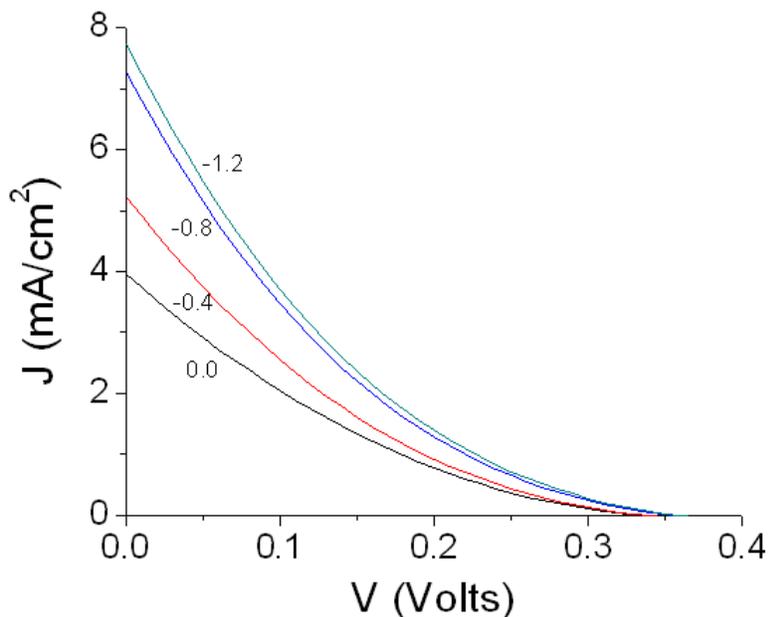


Figure S5. Experimental IV plots for type B “bilayer” graphene (two monolayers) on n-type Si ($N_D \sim 10^{16}/\text{cm}^3$). Performance improves as the gate voltage (curve labels) is varied from $V_g = 0.0$ V to -1.2 V. The consistently lower V_{oc} (relative to the monolayer case, main text Fig. 4) may be partly due to limiting of the gate effect by folds introduced during application of the second layer.

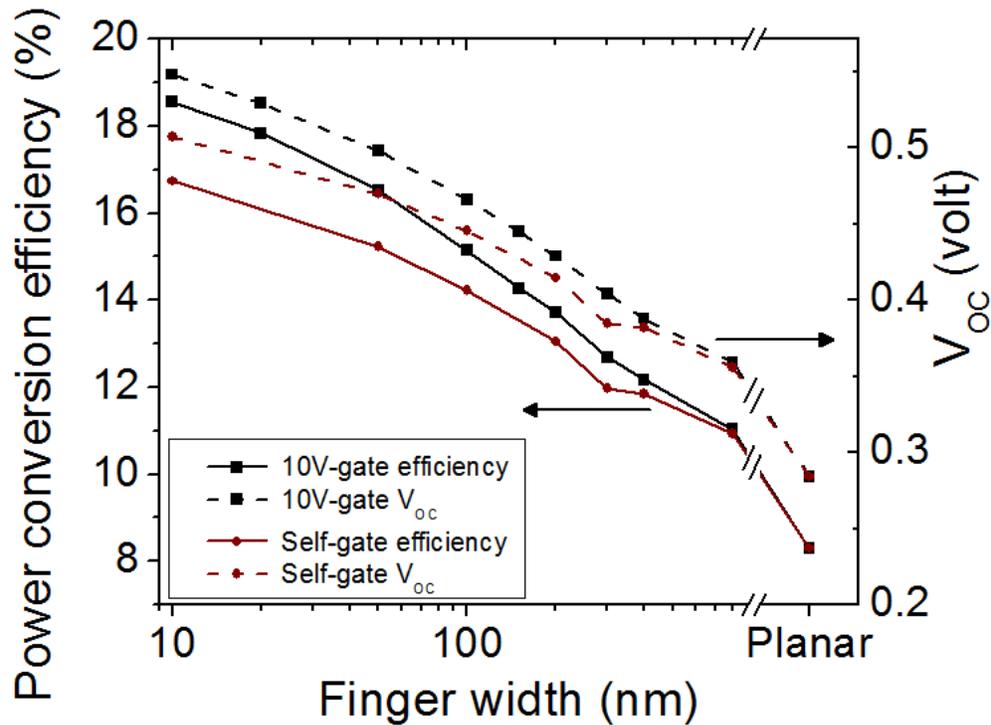


Figure S6. Comparing self-gating and saturated gating for type A devices. Simulations of maximum PCE for various self-gated and non-self-gated configurations for Schottky type A devices. We observe that the self-gating configuration can achieve nearly the same ultimate efficiencies as those with a saturated external gate.

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